IN THE CLAIMS

Claims 1, 2, 4-7, 10-12, 14-19, 22-23, and 27-33 are pending. No claims have been amended. A complete list of claims is presented below for the convenience of the Examiner:

1. (Previously presented) An apparatus comprising:

a processor interface unit; and

a cache to store information received from a processor coupled to the processor interface unit, the cache to store disposable information that may be overwritten without ever having delivered the disposable information to a system memory if the disposable information has been read at least once, the cache further including a cache management unit to determine whether a cache entry contains disposable information by comparing a disposable information cache entry address with a range of addresses that define a disposable information address space.

2. (Original) The apparatus of claim 1, the cache to further store non-disposable information.

3. Cancelled.

4. (Previously presented) The apparatus of claim 2, further comprising a bus interface unit to allow a device coupled to the bus interface unit to access the cache.

5. (Previously presented) The apparatus of claim 4, the cache management unit to allow the cache entry to be overwritten once the device coupled to the bus interface unit reads the cache entry and if the cache management logic determines that the cache entry contains disposable information.

6. (Original) The apparatus of claim 5, further comprising a system memory controller.

7. (Original) The apparatus of claim 6, the cache management unit to cause the cache entry contents to be delivered to the system memory controller for delivery to a system memory if the cache management unit determines that the cache entry does not contain disposable information.

8. Cancelled.

9. Cancelled.

10. (Previously presented) The apparatus of claim 7, further comprising at least one programmable register to store addresses that define a disposable address space.

11. (Previously presented) A system, comprising:

a processor; and

a system logic device coupled to the processor, the system logic device including

a processor interface unit, and

a cache to store information received from a processor coupled to the processor interface unit, the cache to store disposable information that may be overwritten without ever having delivered the disposable information to a system memory if the disposable information has been read at least once, the cache further including a cache management unit to determine whether a cache entry contains disposable information by comparing a disposable information cache entry address with a range of addresses that define a disposable information address space.

12. (Original) The system of claim 11, the cache to further store non-disposable information.

13. Cancelled.

14. (Previously presented) The system of claim 12, the system logic device further including a bus interface unit.

15. (Original) The system of claim 14, further comprising a device coupled to the system logic device bus interface unit.

16. (Previously presented) The system of claim 15, the cache management unit to allow the cache entry to be overwritten once the device coupled to the bus interface unit

reads the cache entry and if the cache management logic determines that the cache entry contains disposable information.

17. (Original) The system of claim 16, the system logic device further including a system memory controller.

18. (Original) The system of claim 17, further comprising a system memory coupled to the system memory controller.

19. (Original) The system of claim 18, the cache management unit to cause the cache entry contents to be delivered to the system memory controller for delivery to the system memory if the cache management unit determines that the cache entry does not contain disposable information.

20. Cancelled.

21. Cancelled.

22. (Original) The system of claim 21, the system logic device further including at least one programmable register to store addresses that define a disposable address space.

23. (Previously presented) A method, comprising:

receiving a line of information from a processor;

storing the line of information in a cache;

determining whether the line of information is disposable by comparing the address of the line of information with a range of addresses that defines a disposable information address space; and

overwriting the line of information, if it is determined to be disposable, without ever having written the line of information to a system memory once the line of information has been read by a system device.

24. Cancelled

25. Cancelled.

26. Cancelled.

27. (Previously presented) An apparatus comprising:

a processor interface unit; and

a cache to store information received from a processor coupled to the processor interface unit, the cache to store disposable information that may be overwritten without ever having delivered the disposable information to a system memory if the disposable information has been read at least once, the processor interface unit to receive a disposable information attribute indication from the processor when the processor delivers the disposable information to the processor interface unit.

28. (Previously presented) The apparatus of claim 27, the cache to further store non-disposable information.

29. (Previously presented) The apparatus of claim 28, further comprising a bus interface unit to allow a device coupled to the bus interface unit to access the cache.

30. (Previously presented) The apparatus of claim 29, the cache management unit to allow the cache entry to be overwritten once the device coupled to the bus interface unit reads the cache entry and if the cache management logic determines that the cache entry contains disposable information.

31. (Previously presented) The apparatus of claim 30, further comprising a system memory controller.

32. (Previously presented) The apparatus of claim 31, the cache management unit to cause the cache entry contents to be delivered to the system memory controller for delivery to a system memory if the cache management unit determines that the cache entry does not contain disposable information.

33. (Previously presented) A method, comprising:

receiving a line of information from a processor;

storing the line of information in a cache;

determining whether the line of information is disposable by examining an attribute communicated along with the line of information by the processor; and

overwriting the line of information, if it is determined to be disposable, without ever having written the line of information to a system memory once the line of information has been read by a system device.